IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-27. (Canceled)

28. (Currently Amended) A semiconductor memory device comprising:

a semiconductor element;

a plurality of lead wires connected to a plurality of connecting electrodes formed on said semiconductor element;

at least a single dummy lead wire that is not electrically connected to said semiconductor element and does not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;

an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening portion of said insulating film,

wherein said at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, the two adjacent lead wires being provided on one side of the insulating film to define the space on the one side of the insulating film ~~and~~

~~wherein at least two adjacent dummy lead wires provided on one side of said insulating film have tip portions connected to each other on the semiconductor element~~.

29. (Currently Amended) A semiconductor memory device comprising:

a semiconductor element;

a plurality of lead wires connected to a plurality of connecting electrodes formed on said semiconductor element;

at least a ~~single~~ pair of dummy lead ~~wire that is~~ wires that are not electrically connected to said semiconductor element and ~~does~~ do not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;

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an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the ~~single~~ pair of dummy lead ~~wire~~ wires; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the ~~single~~ pair of dummy lead ~~wire~~ wires within the opening of said insulating film,

wherein ~~said at least a single dummy lead wire is~~ one and the other of said at least the pair of dummy lead wires are provided on one side and an opposite side of said insulating film, respectively, each of the one and the other of said at least the pair of dummy lead wires being arranged in ~~a space~~ corresponding first and second spaces defined by first and second two adjacent lead wires of said plurality of lead wires, respectively, so that a length of each said ~~space~~ first and second spaces is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, said first two adjacent lead wires being provided on said one side of said insulating film to define said first space on said one side of said insulating film, and said second two adjacent lead wires being provided on said opposite side of said insulating film to define said second space on said opposite side of said insulating film ~~and~~

~~wherein a dummy lead wire is formed on each of two opposing sides of said~~

D1 ~~semiconductor element and tip portions of the dummy lead wires positioned to face each~~

~~other are connected to each other to form a straight single dummy lead wire~~.